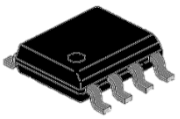
SQ7131/SQ7133/SQ7135
Brief Datasheet V1.8

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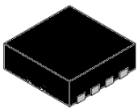
SQ7131/SQ7133/SQ7135

Low Power Secure ASIC, ECC-256, ECDSA, ECDH, AES-128/AES-256, SHA 256, TRNG

- Basic Information
  - Operating Voltage : 2.0V ~ 5.5V
  - Operating Temperature : -40°C ~ 85°C
- Security Features
  - Asymmetric H/W Accelerator
    - NIST Standard P-256 Elliptic Curve Support
    - ECDSA: FIPS186-4 Elliptic Curve Digital Signature
    - ECDH: FIPS SP800-56A Key Agreement
  - Symmetric H/W Accelerator
    - FIPS 180-4 SHA-256 & FIPS 198-1 HMAC Hash Algorithm
    - FIPS-197 AES-128/256: Encrypt/Decrypt, Galois Field Multiply for GCM
  - Networking Key Management Support
    - KDF-PRF/AES/HKDF Calculation for TLS 1.2 & 1.3
    - ECDHE : Ephemeral key generation and key agreement
  - True Random Number Generator(TRNG)
  - Active Tamper Detection
  - Simple/Differential Power Analysis Attack Countermeasure (SPA/DPA)
  - Independent Internal Clock to Prevent Glitch Attack
  - 128-bit Unique UID
- Certification
  - NIST CAVP : DRBG, AES, SHA2, ECDSA and HMAC
  - NIST ESV Certified and CMVP FIPS 140-3 Complied
  - STQC Level 2 certified
  - SESIP & PSA Level 3 certification ready
- Package



SOP8



8-Lead DFN (3mm x 3mm)

- Secure Storage
  - Chip-Dependent Encryption Technology
  - Secure Storage for Key, X.509 Compressed Certificate, Data
  - Large User Data Storage : 5.6KB
- Communication Interface
  - SQ7131 supports standard I2C (Max: 1MHz)
  - SQ7133 supports standard SPI (Max: 10MHz@MODE3)
  - SQ7135 supports SWI (Single Wire Interface) (230.4Kbps)
- Applications
  - Accessory Authentication
  - System Anti-Cloning
  - End-to-End Encryption
  - Secure TLS 1.2 and 1.3 Communication
  - AIoT Device Security
  - Secure Boot /Secure OTA

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1. Preface

SQ713x supports many hardware cryptographic accelerators: embedded high-quality TRNG (True Random Number Generator), SHA-256, asymmetric encryption ECC-256, and symmetric encryption AES-128/AES-256. It also has secure storage for ECC and AES keys storage.

The device is suitable for building high-security applications, such as IoT symmetric/asymmetric authentication, attestation, TLS1.2/1.3 secure connections, secure boot, secure OTA, and F/W protection, etc.

Secure storage for ECC and AES keys:

Key Type	SQ713x	Note
AES Key (AES-128/256)	12	Slot 8~19
ECC Private Key – 256	7	Slot 1~7
ECC Public Key – 256	4	Slot 24, 26~28

Table 1-1 AES and ECC Key Slots

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2. Pin Assignment/Description

2.1 SQ7131 Pin Assignment/ Description

PRODUCT: SQ7131SP008C00R

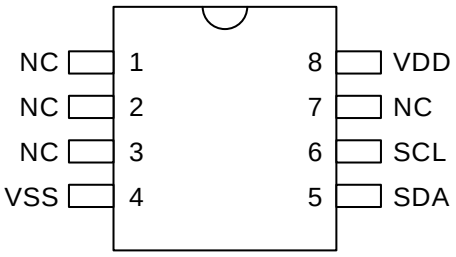


Figure 2-1 Pin Assignment of SQ7131 SOP8

PRODUCT: SQ7131N3008C00R

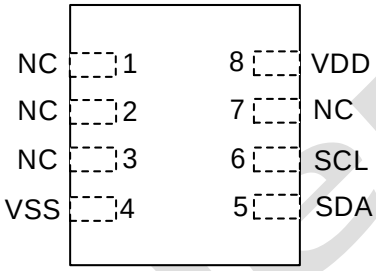


Figure 2-2 Pin Assignment of SQ7131 8-Lead DFN

Pin No.	Pin Name	I/O Type	Description
1	NC	-	No Connect
2	NC	-	No Connect
3	NC	-	No Connect
4	VSS	GND	Ground
5	SDA	I/O	I2C Serial Data
6	SCL	I	I2C Serial Clock Input
7	NC	-	No Connect
8	VDD	Power	VDD power Supply

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2.2 SQ7133 Pin Assignment/Description

PRODUCT: SQ7133SP008S00R

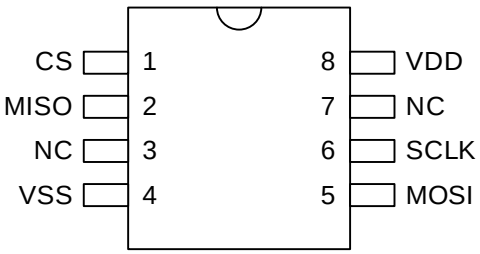


Figure 2-3 Pin Assignment of SQ7133 SOP8

PRODUCT: SQ7133N3008S00R

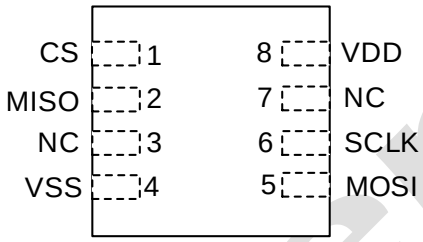


Figure 2-4 Pin Assignment of SQ7133 8-Lead DFN

Pin No.	Pin Name	I/O Type	Description
1	CS	I	SPI, Chip Select
2	MISO	O	SPI, Master In Slave Out
3	NC	-	No Connect
4	VSS	GND	Ground
5	MOSI	I	SPI, Master Out, Slave In
6	SCLK	I	SPI, Clock Input
7	NC	-	No Connect
8	VDD	Power	VDD power Supply

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2.3 SQ7135 Pin Assignment/Description

PRODUCT: SQ7135SP008W00R

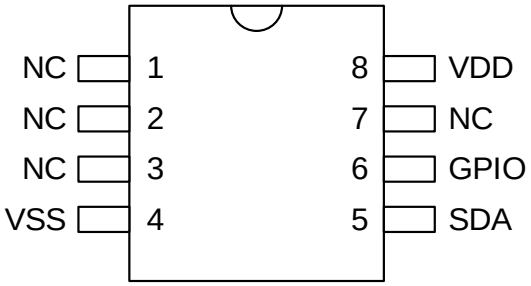


Figure 2-5 Pin Assignment of SQ7135 SOP8

PRODUCT: SQ7135N3008W00R

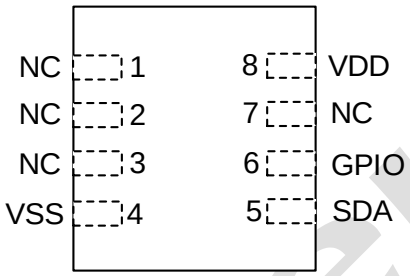


Figure 2-6 Pin Assignment OF SQ7135 8-Lead DFN

Pin No.	Pin Name	I/O Type	Function Description
1	NC	-	No Connect
2	NC	-	No Connect
3	NC	-	No Connect
4	VSS	GND	Ground
5	SDA	I/O	SWI, single wire input/output pin
6	GPIO	I/O	General purpose input/output
7	NC	-	No Connect
8	VDD	Power	Positive Power Supply

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3. Electrical Characteristics

3.1 Absolute Maximum Rating

The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

(Vss=0V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}	-	-0.3 to 6.0	V
Input Voltage	V_{IN}	All I/O pins	-0.3 to VDD+0.3	V
Output Current(Total)	I_{OL}	All I/O pins	100	mA
Storage Temperature	T_{STG}	-	-50 to 125	℃

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3.2 Operation Conditions

The following defines the electrical characteristics of the device when it is operated at voltage and temperature maximum/minimum values. Unless otherwise stated, the standard conditions were determined at "operating temperature 25°C and operating voltage VDD = 3.3 V."

3.2.1 Operation Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}		2.0	3.3	5.5	V
Operating Temperature	Ta		-40	25	85	℃

3.2.2 I/O Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Low Voltage	V_{IL}	VDD=5V, temperature=25 °C	0		0.3 VDD	V
Input High Voltage	V_{IH}	VDD=5V, temperature=25 °C	0.7 VDD		VDD	V
Output Low Voltage	V_{OL}	VDD=5V, temperature=25 °C IOL= 3 mA	0		0.1 VDD	V
Output High Voltage	V_{OH}	VDD=5V, temperature=25 °C IOH= -3 mA	0.9VDD		VDD	V

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3.3 DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Current in Operation Mode (Note)	IDD_N1	-	3.7	-	mA
Supply Current in Deep Sleep Mode	IDD_DS	-	0.3	-	uA
Supply Current in Operation MODE (During non-ECC Command Execution)	IDD_N2		4.3		mA
Supply Current in Operation MODE (During ECC Command Execution)	IDD_N3		7		mA

Note: The condition is waiting for Commands.

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3.4 Power-on Reset Characteristics

Ta=-40~85℃

Symbol	Description	Min.	Typ.	Max.	Unit
tPPW	Power-on reset minimum pulse width	1	-	-	ms
tPWUP	Warming-up time after a reset is clear and device ready	-	4	-	ms
tVDD	Power supply rise time	0.5	-	5	ms

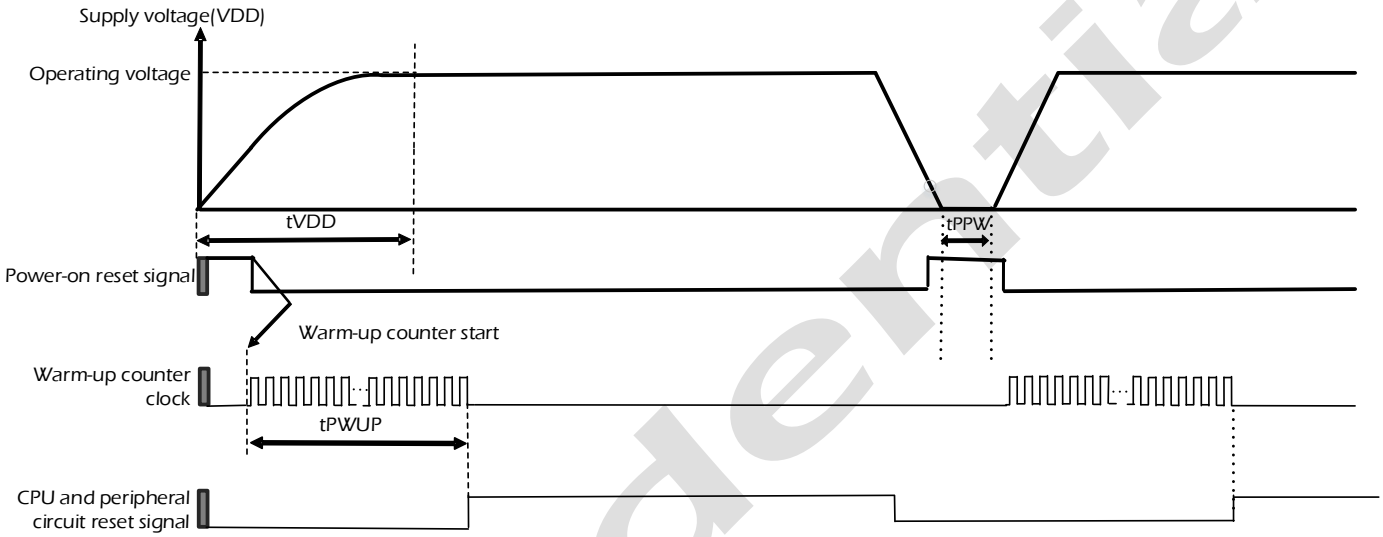


Figure 3- 1 Operation Timing of Power-on Reset

Note：In power-down process, the VDD must be 0V, then re-power-on to ensure the IC operating normal.

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3.5 BROR Characteristics

Ta=-40~85℃

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
BROR detected voltage	VBROR_Falling	VDD fall time > tVDD (for tVDD please refer to CH3.4 Power-on Reset Characteristics)	1.85	1.90	1.95	V

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3.6 AC Characteristics

3.6.1 AC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-Up HW Ready Time	T_{PU_RDY}	-	9.5	-	ms
Power-Up Ready Time – Ready for Command	T_{CMD_RDY}	-	18.5	-	ms
Standby Time, Entering the deep sleep mode	T_{STB}	-	20	-	us
Wake-Up Ready Time, deep sleep mode	Tw_{DS_RDY}	-	2.4	-	ms

Note: The "Typ." value is based on 25°C room temperature, and the Sleep command will change this value.

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3.6.2 I2C Characteristics

Parameter	Symbol	Min.	Max.	Unit
Clock Frequency	f_{SCL}	-	1	MHz
Hold Time Repeated START Condition	$t_{HD;STA}$	0.45	-	us
Low Period of SCL Clock	t_{LOW}	0.65	-	us
High Period of SCL Clock	t_{HIGH}	0.35	-	us
Setup Time for a Repeated START Condition	$t_{SU;STA}$	0.35	-	us
Data Hold Time	$t_{HD;DAT}$	-	0.5	us
Data Setup Time	$t_{SU;DAT}$	0.1	-	us
Rise Time of Both SDA and SCL	t_r	20	300	ns
Fall Time of both SDA and SCL	t_f	20	300	ns
Setup Time of STOP Condition	$t_{SU;STO}$	0.6	-	us
Bus Free Time Between a STOP and START Condition	t_{BUF}	1.3	-	us
Capacitive Load for Each Bus Line	C_b	-	400	pF

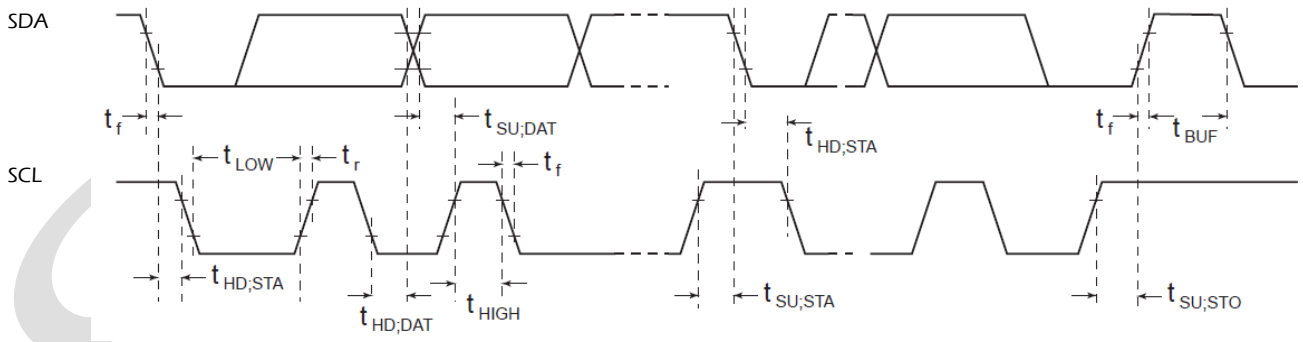


Figure 3-2 I2C Timing Sequence

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3.6.3 SPI Characteristics

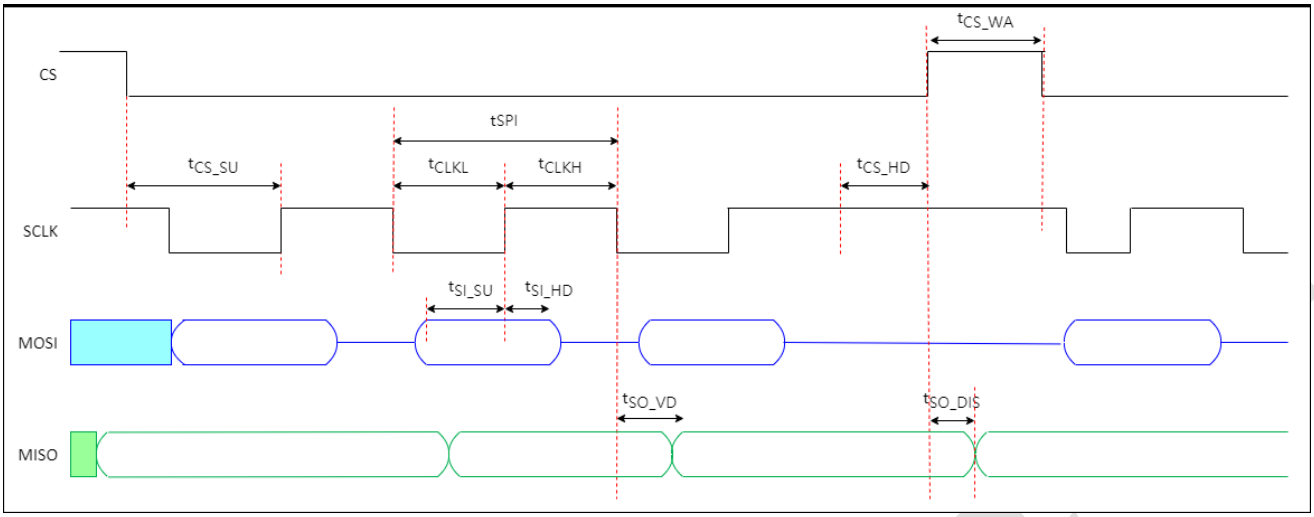


Figure 3-3 SPI Timing Sequence

Parameter	Symbol	Min.	Max.	Unit
SPI Frequency	fSPI	-		
(VDD=2.7V~5.5V, <=55℃)			10	MHz
(VDD=2.7V~5.5V, >55℃)			8	MHz
(VDD=2.0V~2.7V)			5	MHz
SPI Period	tSPI	1/fSPI	-	ns
High period of the SCLK pin	tCLKH	0.4 tSPI	-	ns
Low period of the SCLK pin	tCLKL	0.4 tSPI	-	ns
From SPICS active to first sample edge	tCS_SU	2.0 tSPI	-	ns
From last SCLK shift edge to SPICS inactive	tCS_HD	2.0 tSPI	-	ns
Time between SPI transaction	tCS_WA	3.0 tSPI	-	ns
Data Input Setup Time[1]	tSI_SU	25	-	ns
Data Input Hold time[1]	tSI_HD	10	-	ns
Data Output Valid Time[1]	tSO_VD	-	40	ns
Data Output Disable Time[1]	tSO_DIS	-	25	ns

Note 1: These parameters are characterized but not tested in production.

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3.6.4 SWI Characteristics

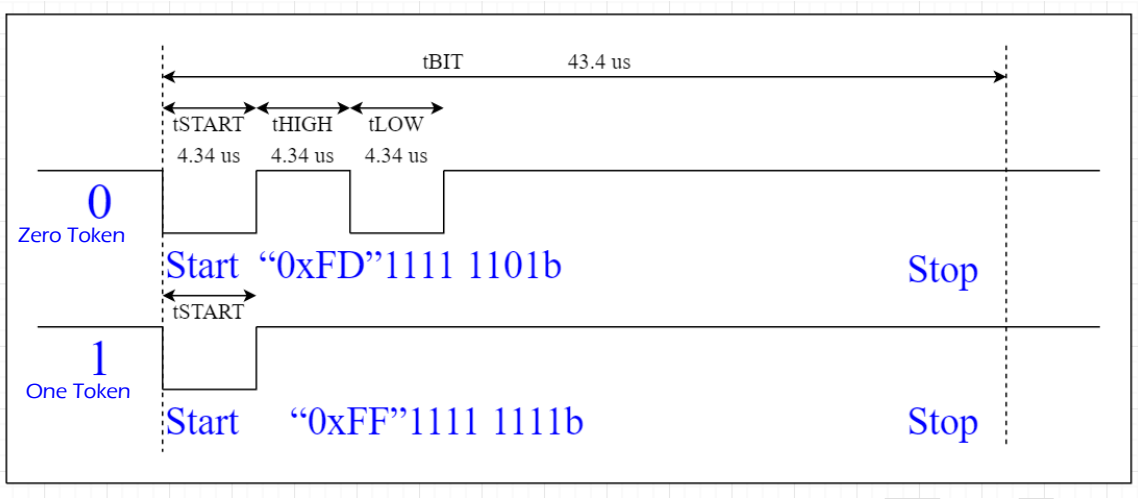


Figure 3-4 SWI Timing Sequence@230.4K (Typ.)

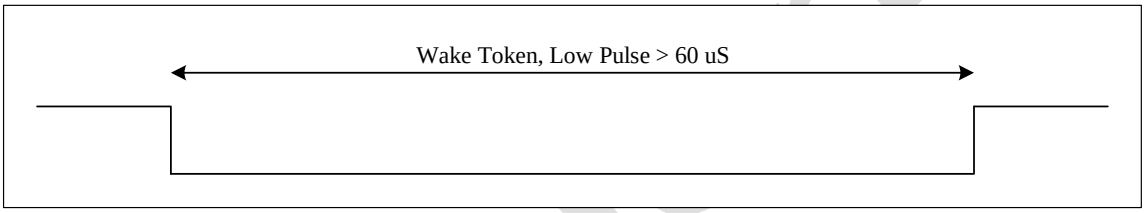


Figure 3-5 SWI Wake Token Timing Diagram

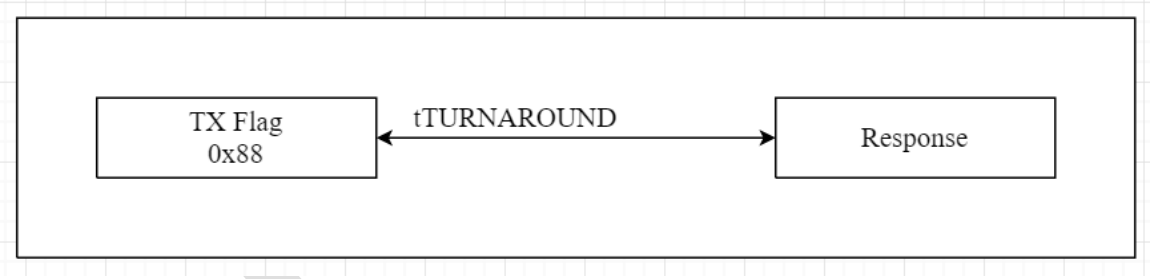


Figure 3-6 SWI Turn Around Timing Diagram

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Parameter	Symbol	Direction[1]	Min.	Typ.	Max.	Unit
Start Token	tSTART	Input	4.10	4.34	4.56	μs
		Output	3.91	4.34	4.77	μs
Data Token High	tHIGH	Input	4.10	4.34	4.56	μs
		Output	3.91	4.34	4.77	μs
Data Token Low	tLOW	Input	4.10	4.34	4.56	μs
		Output	3.91	4.34	4.77	μs
Bit Time[2]	tBIT	Input	41	43.4	46	μs
		Output	39	43.4	48	μs
Turn Around[3]	tTURNAROUND	Input	10	-	-	μs
		Output	86	96	106	μs
Bus Timeout[4]	tTIMEOUT	Input	65	-	-	ms

Note 1: Direction is with respect to SQ713x device. Input is from Master to SQ713x, Output is from SQ713x to Master.

Note 2: Bit Timing: tSTART, tLOW, tHIGH, and tBIT are designed to be compatible with a standard UART baud rate at 230.4 kbps. The UART is set to one start bit, eight data bits, no parity and one Stop bit.

Note 3 : Turnaround time: SQ713x will initiate the first output low going transition after this time interval following the initial falling edge of the start pulse of the last bit of the transmit flag. After SQ713x transmits the last bit of a group, system must wait this interval before sending the first bit of a flag. It is measured from the falling edge of the start pulse of the last bit transmitted by SQ713x.

Note 4: Bus Timeout: SQ713x devices will wait for a Wake Token if the bus is inactive longer than this duration.

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3.7 EEPROM Characteristics

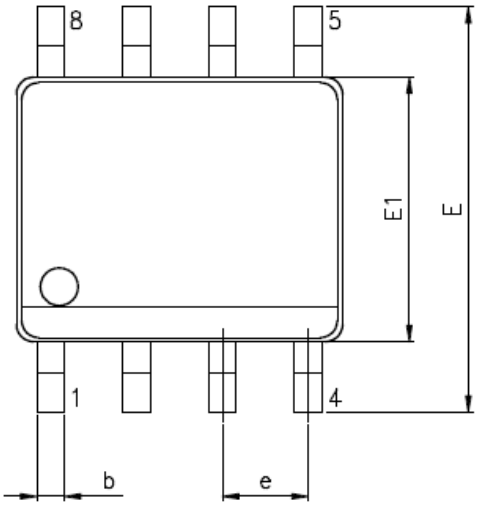
Parameter	Min.	Typ.	Max.	Unit
Write Endurance (Sector Endurance)	100,000	-	-	Cycles
Data Retention(at 25°C)	100	-	-	Years
Data Retention(at 85°C)	20	-	-	Years

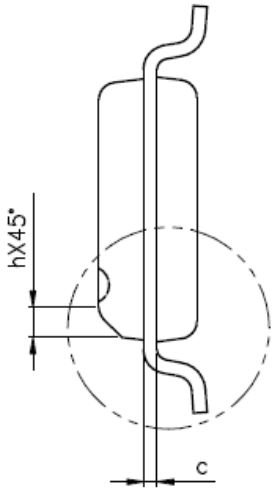
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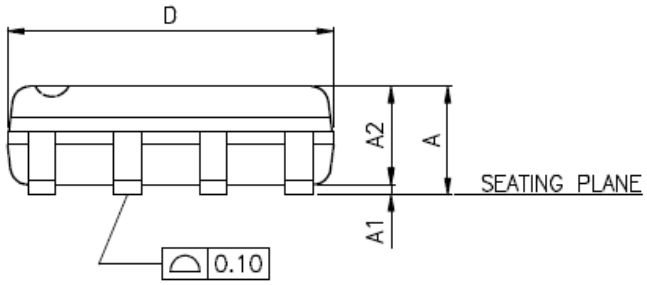
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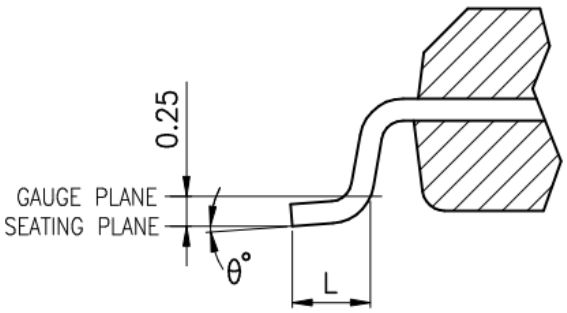
Appendix A. Package Information

SOP8





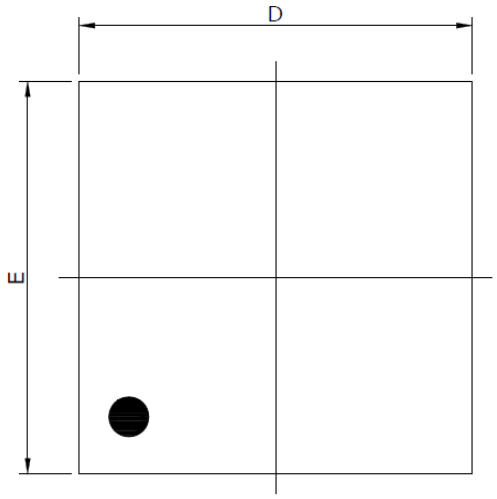




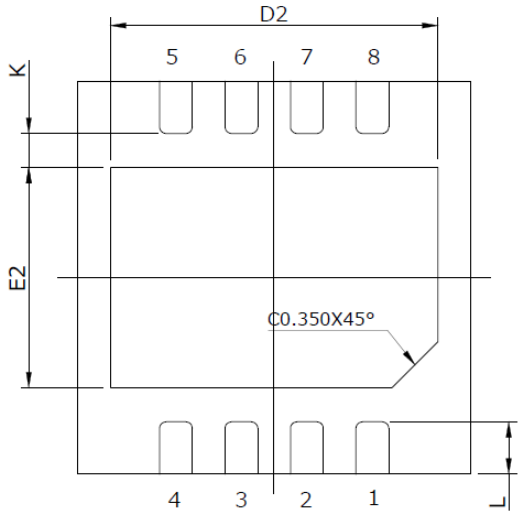
Symbol	mm		
	Min.	Typ.	Max.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
L	0.40	–	1.27
h	0.25	–	0.50
θ	0°	–	8°

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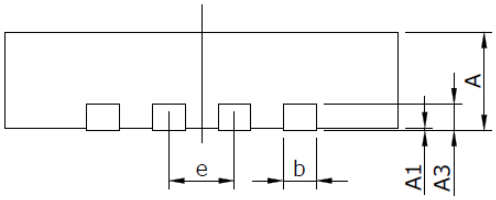
8-Lead DFN (3mm x 3mm)



TOP VIEW



BOTTOM VIEW



Symbol	mm		
	Min.		Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.20	0.25	0.30
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.50 BSC		
L	0.35	0.40	0.45
D2	2.35	2.40	2.45
E2	1.65	1.7	1.75
K	0.20	–	–

Confic

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Appendix B. Ordering Information

When ordering products, please provide the following details:

Ordering Information	Product	Packing	Provisioning Service	Description
Example	SQ7131SP008C00R	T	Y	I2C, SOP8, Tape & Reel, 85℃, provisioning service
	SQ7131N3008C00R	B	N	I2C, DFN 3x3, Tray, 85℃, no provisioning service
	SQ7133SP008S00R	B	Y	SPI, SOP8, Tube, 85℃, provisioning service
	SQ7133N3008S00R	T	N	SPI, DFN 3x3, Tape & Reel, 85℃, no provisioning service
	SQ7135SP008W00R	B	Y	SWI, SOP8, Tube, 85℃, provisioning service
	SQ7135N3008W00R	T	N	SWI, DFN 3x3, Tape & Reel, 85℃, no provisioning service

Note 1: "Packing"- T: Tape & Reel; B: Tube/Tray

Note 2: "Provisioning service for Customers"- Y: Need provisioning service for customers; N: No need for provisioning service from customers

Note 3: For Packing T, SOP: 4K/Reel, DFN: 5K/Reel

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Appendix C. Product Number Information

Example : **SQ 71 31 SP 008 C 00 R T Y**

iMQ SQ product

Product Series

Sub Series

Package Type

Code	Package Type
SP	SOP
N3	DFN 3x3

Pin Count

Code	Pin
008	8

Communication Interface

Code	Type.
C	I2C
S	SPI
W	SWI

Designator

Operating Temp

Code	Operating Temp.
R	-40~85°C

Packing

Code	Packing
T	T&R
B	Tube

Provisioning Service

Code	Provisioning
Y	Yes
N	No

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Revision History

Version	Approved Date	Description
V1.8	2025/10/17	1. Sync with full datasheet V1.8
V1.7	2025/08/05	1. In Appendix B. Ordering Information, add Note 3 2. In Appendix B. Ordering Information, modify Packing "T" to "B" and the related descriptions in SQ7131N3008C00R, SQ7133SP008S00R, and SQ7135SP008W00R
V1.6	2025/04/23	1. Sync with full datasheet V1.6
V1.5	2024/04/18	1. Add SQ7135 SWI (Single Wire Interface) info
V1.4	2024/03/05	1. Add Appendix B. Product Number Information 2. Add "tSPI" in 3.6.3 SPI timing figure
V1.3	2023/12/14	1. Sync with full datasheet V1.3
V1.2	2023/11/02	1. Sync with full datasheet V1.2
V1.1	2023/05/24	1. Sync with full datasheet V1.1
V1.0	2023/01/18	1. Sync with full datasheet V1.0
V0.7	2022/09/19	1.1st version issue

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